



Maximize high-speed signal integrity with the right choice of cables, layout, and equalizer ICs (Part 2)

By Eric Sweetman, Senior Applications Engineer, Vitesse Semiconductor Corp.

[Planet Analog](#)

Feb 02, 2009 (7:00 AM)

URL: <http://www.planetanalog.com/showArticle?articleID=212903426>

Editor's Note: Previous parts of this multipart article include:

Part 1 examines the basic problems of high speed signals, PCBs, cables, and backplanes, click [here](#). There are also additional relevant items of interest listed and linked at the end, below the *About the author* section.

Introduction

A few key principles can guide the development of PCBs and backplanes. These are based on some key characteristics of high-speed signal behavior and responses:

- *First* is the deterministic nature of the loss. These losses are predictable, non-random behavior that can be simulated and prototyped with a high degree of confidence. Simulations can be of significant value in board and system design, but do not always include significant factors such as metal surface finish and dielectric losses. As a result, it is easier to match simulation to measured data after you have measured it.
- *Second*, signal-integrity engineering requires attention to some details that are not obvious at first. As an example, solder-pad capacitance may become of utmost importance during system bring-up, whereas it may have been overlooked during system development.
- *Third*, the losses are of reasonable scope and do not strongly challenge the electronics. The dynamic range of signal loss in most cases is about 30 dB or less. This dictates the type of electronics required to deal with signal loss.

This is important in high-speed system design. If up to 20 dB of loss can be budgeted in a design, inexpensive electronics are available to handle the loss. However, if loss is up to the 40 dB range, much more sophisticated electronics will be needed to address the level of loss factor. These would become much more challenging projects to deal with 100:1 ratio in signal amplitude from low-to-high frequency, which is much more costly to address. So, keep loss to about 20 dB, and your pocketbooks will be happy.

The loss is measured at a frequency of half the data clock rate. For example, a 2 Gbps path-loss measurement should be measured at 1 GHz and below. It is important to look at the shape of the loss curve. Most parts can handle a smooth, monotonic loss curve well, but if there is much structure in the loss curve, it is much harder to equalize.

One simple principle: manage your discontinuities!

Discontinuities are the key element that separates the level of semiconductor technology required to deal with signal integrity. If discontinuities are properly managed and minimized, there are simple, low-cost electronic and IC solutions to help solve your problem. If the signal path has several discontinuities, reflections, echoes, and crosstalk effects, then complexities will go up resulting in significantly longer development time and higher costs.

So, how do you design for success? The following three rules set the stage for proper layout design to enable multi-Gbps signals:

- Keep it Simple
- Loss is Not the Problem
- Discontinuity Budget = 1

After numerous customer-layout design reviews conducted at Vitesse, these three rules applied above all others in addressing recurring issues in problematic designs.

Keep it Simple: The idea behind keeping it simple is that overcomplicated designs can wreak havoc on the end goal of a design. In this case, it's getting a high-speed signal from point "a" to point "b." Wrapping too much complexity in a design will lead to a compounded complexity effect. This is especially true when interfacing high-speed I/O macros from different vendors over complex terrains. Complicated signal paths will lead to complicated frequency responses, which will lead to more costly, complicated ICs.

Loss is Not the Problem: A well-designed IC has enough gain to recover a significantly attenuated signal. Do not worry about the loss. A common question would arise from customers: how many inches of copper can you equalize? There is no set answer to this question due to variations in material, environment, humidity conditions, etc., which will also affect signal path.

In the big picture, however, the loss does not matter due to deterministic nature and if reasonable in scope; equalizers can address this loss. In short, if an interconnect/ PCB designer can control discontinuities, equalizers will handle the loss within reasonable boundaries.

Discontinuity Budget = 1: Discontinuities are not conducive to high-speed signals, but designers are allowed one bad discontinuity. A properly terminated path can absorb a single massive glitch located anywhere.

If destination is properly terminated, ping-pong like reflections will be avoided aiding designs to the high-GHz range. The following are examples of what is "OK" and "Not OK" in terminations: **Figure 2.1** and **Figure 2.2** show a properly source-terminated transmission lines.

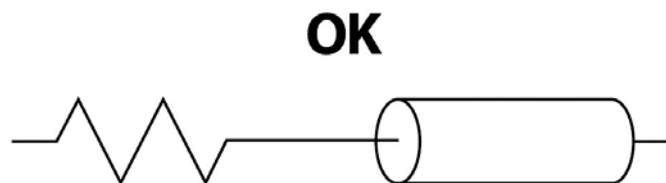


Figure 2.1: Properly terminated path

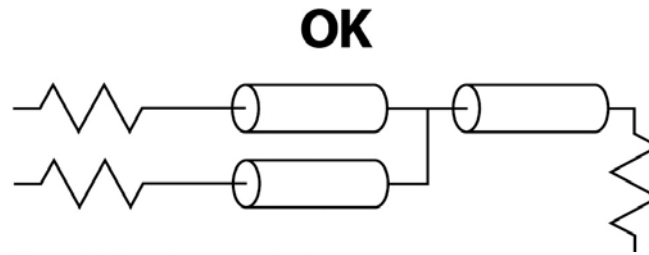


Figure 2.2: Properly terminated path

You cannot do as is shown in **Figure 2.3**, where an open stub creates discontinuity, reflections, and standing waves.

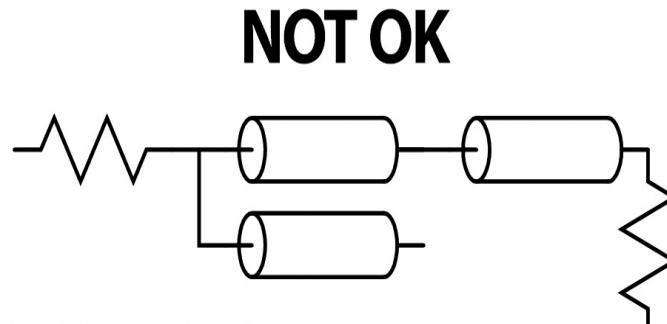
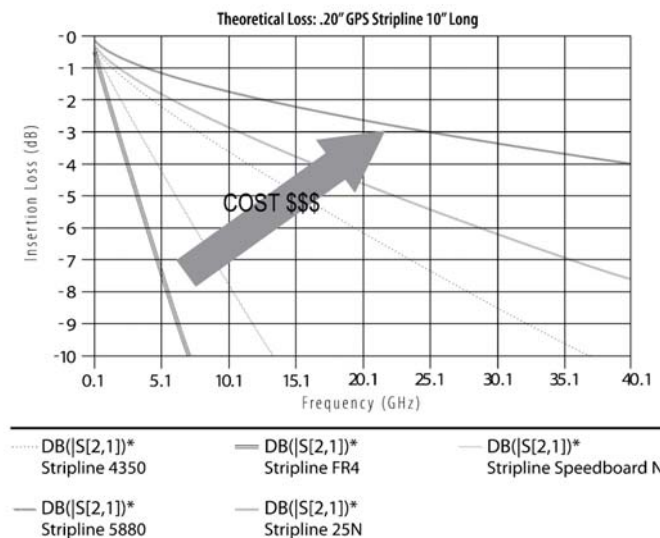


Figure 2.3: Improperly terminated path

This greatly complicates the equalization techniques needed to counter these effects.

Choosing PCB Material

Board materials can reduce loss, but at a great cost. The graph of **Figure 2.4** shows loss curves of striplines based on different PCB materials. When looking at these curves, it is important to look at frequency up to the 40 GHz range, and to realize that even the lowest-cost materials have manageable loss characteristics. The 'worst case' curve shows loss of -10 dB in the 5 GHz range (equates to 10 Gbps), which is reasonable for equalizer circuits.



*Figure 2.4: Theoretical loss
(Click on image to enlarge)*

The difference in cost for these materials can be spectacular. Standard FR-4, or a notch up like Nelco 4000, will more than likely do the job when paired with reasonable equalization circuits.

Also note the importance of manufacturability. With the transition to Pb-free and RoHS-compliant materials, board materials are going to be stressed due to reflow profile differences and higher temperatures. So, some of the more expensive, exotic materials could also become less manufacturable once the lead-free transition kicks in. Our advice is put your money somewhere other than expensive PCB materials.

Transmission Line Design Guidelines

Ground Via Spacing

After years of experience in designing multiple high-speed boards, we realized the important issue of ground-stitch via spacing. This means making sure that when signals propagate down the transmission lines, there are no alternative propagation (or waveguide) modes. These can occur based on how well a grounded environment is maintained for the signal propagation.

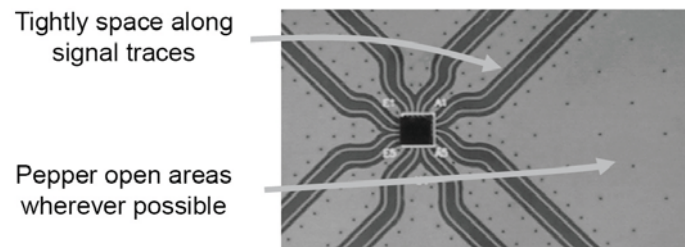
Waveguide Modes:

- Can develop between ground vias
- Can affect loss and create resonances

Fill with Via:s

- Keep spacing within a fraction of wavelength
- Consider 3rd harmonics

Figure 2.5 shows an example of tightly spaced ground vias along the edge of differential pairs. The large copper fill area is also enhanced with ground vias.



*Figure 2.5: Tightly spaced ground vias
(Click on image to enlarge)*

Figure 2.6 shows the recommended via spacing based on data rate. Since some spacings are not always practical, one option is to have the layout designer approach it as if doing copper fill, then go back and look at where they can put in vias. If this cannot be done, it is better to remove copper fill than leave it unstitched. We have observed boards resonate due to improper copper-fill issues.

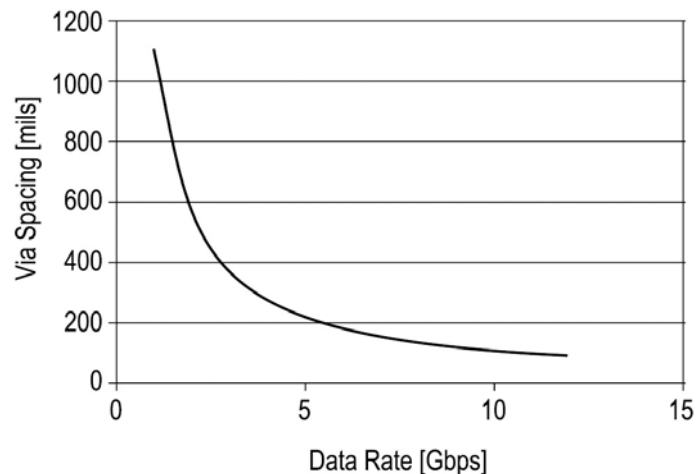


Figure 2.6: Recommended via spacing based on data rate
(Click on image to enlarge)

Ground plane clearance for vias

With complex circuit boards, the thickness of the board is a significant fraction of the wavelength at high data rates. As a signal passes through a via to the other side of a board or to a different layer in a board, it is important to have the via impedance as close as possible to 50 Ω to minimize reflections.

In general, recommended ground-via cutouts will result in via impedance significantly lower than 50 Ω . Electromagnetic field simulation programs are often used to design via diameter and cutouts to minimize impedance discontinuities. In this section, we discuss an easy technique to estimate the appropriate ground plane clearance to provide close to 50 Ω characteristic-impedance vias.

The primary assumption we make for estimating via ground-plane clearance is that the via is the center conductor of a coaxial transmission line and the ground planes represent the shield of the transmission line. While one might assume that since the ground planes are not a continuous cylinder of copper, the ground planes may be significantly closer to the via than for a similar coaxial transmission line. The main reason the spacing should be comparable to a coaxial line is that the capacitance at the edges of the plane have fringing capacitance that is close to that of a continuous cylinder.

Next, we calculate the appropriate size ratio for the via diameter to ground plane cutout. The equation for the impedance of a coaxial transmission line shows impedance is proportional to the logarithm of the ratio of inner diameter to outer diameter. The characteristic impedance equation for a coaxial line is:

$$Z_0 = (138/\sqrt{E}) \times \log (\text{outer diameter}/\text{inner diameter})$$

where Z_0 is the characteristic impedance, E is the relative dielectric constant, outer diameter is the diameter of the shield and inner diameter is the diameter of the center conductor. Note that the units for diameters do not need to be specified, they will cancel out; the inner and outer diameter need only be in the same units

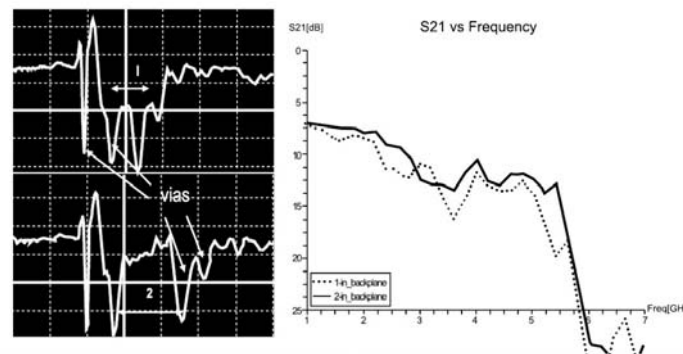
The relative dielectric constant is also a factor. For a circuit board with a relative dielectric constant of 4, a ratio of 1:5 for the inner to outer diameter results in 48 Ω characteristic impedance. For example, an 8-mil diameter via (8 mils is the diameter of the outside of the metal forming the via) should have a 40-mil diameter cutout in the ground planes, to get a characteristic impedance of 48 Ω .

When the above exercise is applied to real boards, it is readily apparent that providing a 1:5 ratio for the via to plane cutout is difficult. Most layouts use significantly smaller ground plane cuts and as a consequence have significantly less than 50-ohm impedance for vias.

Discontinuities should drive board design and layout considerations

There are fairly simple steps one can take to clean up a signal path. Managing discontinuities is the key guiding principle in this process, so special attention and awareness of where and which discontinuities exist in a signal path is needed. This management will help you avoid crossing the 20-dB loss threshold and will result in lower cost and a design that is easier to implement.

As an example, the TDR data in **Figure 2.7** was taken from a production backplane.



*Figure 2.7: Discontinuities due to backplane connector vias
(Click on image to enlarge)*

Running a signal through the backplane, a clean path would have resulted in the 'dotted line' shown on the right-hand diagram. However, discontinuities due to backplane connector vias disrupt the real world result. Factors like airflow, form factor, line card pitch, and board thickness result in discontinuities and impact the end result. As the figure shows, the two discontinuities spaced 200 to 400 psec apart resulted in a capacitive glitch creating a two-pole filter and steep roll-off as shown on the right.

In this case, there is an optimal scenario of having steep roll-off. A worst-case scenario would be a steep notch with the signal coming back again. This type of multiple discontinuity comes up in many backplanes.

PCB Design Review Checklist

Below is a simplified checklist of what to look for in PCB design. These miscellaneous rules will help minimize signal integrity issues. These are must-haves in doing schematic reviews.

Schematic:

- Spread out bypass capacitor values, eg: 0.01/0.1/1.0 μF
- Eliminate blocking capacitors wherever possible

For bypass capacitors, the common rule is to spread out values used in the design. It is important to NOT just use a single value. A common problem in designs is the use of only 0.1 μF capacitors in a design, but you need to spread values from 0.01 μF to 1 μF . The reason for spreading these values is that a bypass cap has a complex frequency response with resonance, and will go inductive above a certain frequency.

By choosing different values, you can spread out frequency notches and the associated power distribution system (PDS) response. This will flatten impedance, creating more of a broadband decoupling network.

Another place we have seen difficulties is based on the data pattern being put into the chip. The repetition rate of pattern has low-frequency content, such as the framing sequence in 8B/10B idle patterns. A framing sequence in a SONET/SDH signal, for example, can cause a short-term lower-frequency wobble in waveform that may not be properly decoupled by the power supply. When that happens, additional noise interactions occur that may not have been anticipated.

Blocking capacitors are becoming less important based on the termination capabilities of semiconductors. These are, however, still advisable in environments with multiple power-supply domains, and are required by some data standards.

In more and more cases, semiconductor terminations allow for removal of these blocking capacitors. This allows going from one component through a stripline inside the board, straight to the next semiconductor device, eliminating the need to go to the surface, through the blocking cap and back down again. The result is that another unnecessary discontinuity associated with that blocking cap is removed, saving board space and reducing component count.

An important tip in semiconductors is fully differential signal-transmission paths. These are immune to power-supply impedance, but they are sensitive to true/complement skew and offset skew between differential pairs.

Layout:

- Keep lines isolated by spacing at least three dielectric thicknesses
- Avoid or remedy via stubs (Watch spacing between vias relative to data rate)
- Lavish ground vias to prevent modes and resonances
- Cut ground relief under solder pads
- Avoid edge coupling more than 10-20% to minimize skin effect losses
- Matching line lengths between differential pairs by $\sim F20$ psec is usually good enough (Translates to $\sim F100$ mils on most PCBs)

Finally, input-receiver performance is optimized with very high-speed common mode rejection, equivalent to through bandwidth. The true and complement do not have to arrive at the same time, they can arrive skewed with respect to each other and I/O will deal with the signal. The signal can cross the 10/90 % point with no difference to the I/O cell.

This only needs to be managed to cut down on EMI, ground bounce, and noise effects. High-performance semiconductors can handle significant amounts of mismatch. In most cases, there is no need to fine-tune for a 1 microsecond skew.

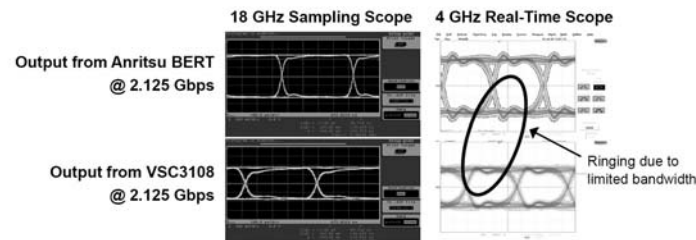
Importance of bandwidth in scopes

In order to understand real-world observations, it is important to understand oscilloscope behavior. Scope readings can be misleading, in some cases, they may even lie to you.

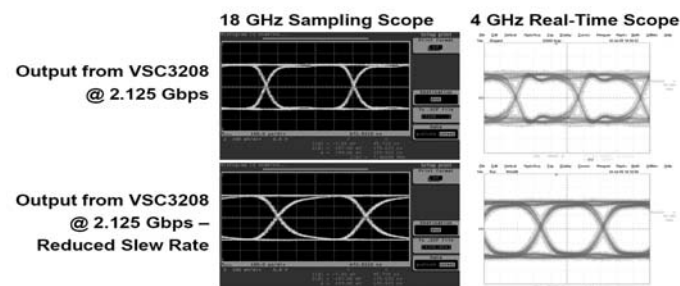
Some digitizing oscilloscopes, in the race to higher speeds, wound up having probe issues. Probing is a difficult design challenge. The probe needs to be on a cable which is 1-meter long, pick up 6 GHz signal, and get from the source to the end point to reconstruct the signal.

To achieve this, manufacturers use some design 'tricks'. A common trick is to set peak response of the amplifier (inserting a zero into the frequency response of the amplifier), which rolls-off skin-effect losses and pushes response back up again. So, the end result is a roll-off in observed response, which introduces resonant response in the scope edge.

We have observed this when doing scope demos and probing signals. We would take the signal of a very-high-performance instrument, such as a Bit Error Rate Tester (BERT), with a very fast edge in the 30 to 40 psec range. The signal would show overshoot and ringing, **Figure 2.8** and **Figure 2.9**.



*Figure 2.8: Misleading reading from oscilloscope
(Click on image to enlarge)*



*Figure 2.9: Correct reading from oscilloscope
(Click on image to enlarge)*

Similarly, this effect can be observed when probing IC outputs. This effect was not an issue until recently. A few years ago, semiconductors from Vitesse and others would put out edge rates in the 100-psec range. Real-time digitizing oscilloscopes coped with these edge rates without issue.

As Vitesse and others started reducing the rise times to about 50 psec, issues crept up. (TDR generators and high-speed pattern generators were generating similar rates.) Some oscilloscopes would then falsely display this ringing effect, when in fact there was none. Your scope should have much-higher bandwidth than the edge rates you plan to observe.

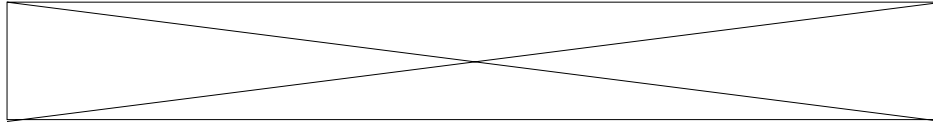
Use the fastest scope available when probing high-speed signals. The key is to make sure that signals and associated harmonics (out to the fifth harmonic) do not surpass the bandwidth of the oscilloscope being used.

About the author

Eric Sweetman, Ph.D., is a Senior Applications Engineer for the Serial Data Solutions Product group at Vitesse Semiconductor Corporation. Eric has worked in various research & development roles covering signal integrity, radio frequency identification (RFID) and Interconnect technologies. Prior to joining Vitesse in 2003, Eric held signal integrity & RFID R&D positions at Accelerant Networks and Lucent Technologies. He holds several patents in RFID technology, along with PhD and MS in physics from the University of Michigan and an SB in physics from MIT.

Related items of interest

- ["An intuitive, practical approach to mixed-signal grounding"](#)
- ["Techniques to enhance op amp signal integrity in low-level sensor applications \(Part 4 of 4\)"](#)
- ["Maintain USB signal integrity when adding ESD protection"](#)
- ["Signal Chain Basics \(Part 21\): Understand and configure analog and digital grounds"](#)



[Copyright © 2003 CMP Media, LLC](#) | [Privacy Statement](#)