

PRODUCT HOW-TO: Keeping Track of the Bandwidth Explosion in Aggregated Video

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The explosion in sources and types of video content is leading to aggregation and management issues in video distribution and broadcasting. This is different issue than end-user display devices home networks.

Professional broadcast video demands including those in video editing and post-production of content are an order of magnitude beyond the end user, or even the cable or telephony service provider.

Two recent trends are exacerbating this problem. The shift from analog film to all-digital movie production has meant that content editors can rely on a uniform base of digital content, but also means that all major movie production efforts are joined with DTV and IPTV production in utilizing a common digital development base.

In addition, the shift to an all-digital broadcast environment in February 2009 may simplify matters from the perspective of abandoning the former dedicated analog systems, but will expand the digital content base which must be managed and monitored.

Studies from the National Association of Broadcasters and independent video analysts predict that the post-February 2009 environment will be characterized by approximately 40,000 local video loops; by 1,745 local TV stations nationwide along with more than 600 national and regional broadcast channels.

Bandwidth demands are escalating even in the present production base, as national HDTV channels grow from a current base of 50 to at least 200 worldwide by 2010. Sporting and entertainment events are pushing towards 1080p resolution, which requires the use of third-generation SDI standards.

In the same way that data networks rely on large core routers in the backbone and multi-gigabit Ethernet switches (or simplified routers) in the data center, the modern video production network is evolving to a two-tiered switching scheme.

The backbone video router, which in legacy applications switched a mix of NTSC, PAL, and SDI signals, is moving to an all-digital crosspoint core, switching SDI and HD-SDI signals. The size of the switching matrix in these core routers is stretching matrix sizes past 500 x 500.

The production studio is moving to the use of an advanced device similar to an audio mixer in a recording studio. This "production mixer" or video switcher may mix legacy analog content, but is optimized for the all-digital source aggregation of the 21st century.

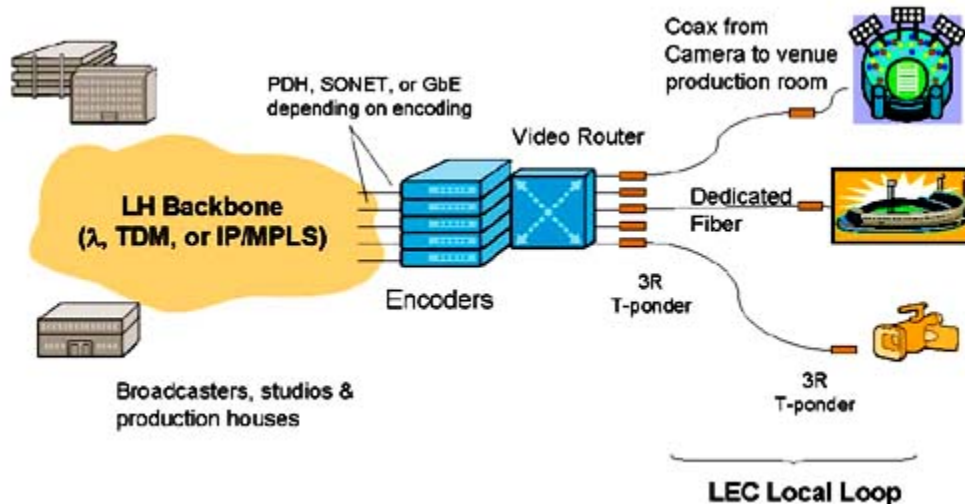


Figure 1: A typical video content acquisition network

What is significant is the degree to which the smaller video switcher is being disseminated into the field. Advances in crosspoint switches, VLSI and in small-footprint transport technology have allowed these switchers to be deployed directly in mobile news vans, and in smaller studios that serve as satellites to the main production and distribution facility.

The initial video feed within the local loop of a local exchange carrier can use fiber or coaxial cable to send a signal to the first level of video switching, after which digital video signals are encoded.

The aggregated stream can then be sent to a primary broadcast studio over a backbone using direct time-division multiplexing (waning but still significant), IP over wavelength, or IP over Multi-Protocol Label Switching protocols (**Figure 1 above**).

Scanning Problems and Solutions

High speed backplane, networking and storage have pioneered concepts for scanning and monitoring high-speed signals. Video aggregation, broadcast and post-production applications can benefit from embedded waveform viewing technology as well.

Like these industries, video transfer bandwidths are moving to multi-gigabit speeds of 3Gbps and above. The arrival of Ultra-High Definition TV in the middle of the next decade may significantly increase bandwidth requirements.

Meanwhile, the move to add advanced signal equalization on-chip has made it difficult to determine signal integrity from traditional eye-diagram analysis. The embedding of dispersion-compensation equalizers within transceivers allowed signals to be recovered from extremely noisy transmissions, but on-chip equalization changes the signal characteristics compared to the signal probed via oscilloscope on the receiver's input.

In a multiple-port switching environment aggregating dozens of video streams, the issue is compounded in analyzing and debug across hundreds of high speed links.

The declining utility of an eye diagram makes the availability of information, and the very notion of using oscilloscopes, problematic at best. One of the reasons test equipment companies developed golden simulators for high-speed signal test was because the traditional eye diagram, which provided the time and amplitude parameters for acceptable bit-error rates, no longer was accessible or meaningful.

As equalization methods improve further, eye diagrams indistinguishable from noise can yield acceptable signals " but they provide no information about the signal conditions.

For development and prototype applications, designers can rely on in-situ probes of the network to capture relevant information. But a real-time video network in the field cannot use in-situ probes, because the intrusion of a probe as a node disrupts the network.

Engineers at Vitesse Semiconductor Corp. recognized this problem early in the decade, and developed patented technologies involving scanning methods for use in high-speed backplanes.

One of these technologies, called VScope, inserts special circuitry in a post-equalization location within the receiver. The method implements scanning blocks within post-equalization clock and data recovery circuitry.

The VScope design deliberately uses the same channel for receiving data and scanning the data eye. The VScope implementation begins with locating the function where the signal transitions from the analog domain to the digital domain.

It is at this location where both analog data (the instantaneous voltage) and the timing information (via clock recovery circuitry) are both present, as illustrated in **Figure 2 below**.

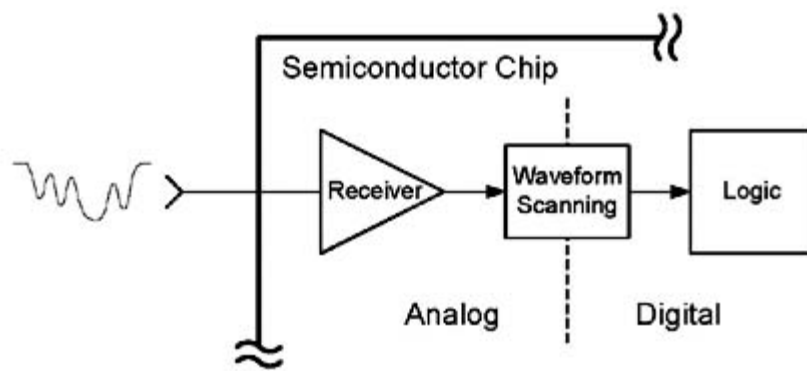


Figure 2. Waveform circuitry is placed in the channel for receiving data and scanning the data eye.

The scanning architecture is based on a dual channel sampling approach that can be inserted directly in the main data path of the input receiver. The core principle of operation is based on gathering two samples of the input data stream, with each sample point adjustable in voltage and time, with a span that covers both the voltage excursion and bit period of the data signal.

The logical result from each sampling channel can be compared on a bit-by-bit basis, and accumulating comparisons over a fixed time period will produce a result similar to a bit-error rate detector as shown in **Figure 3 below**.

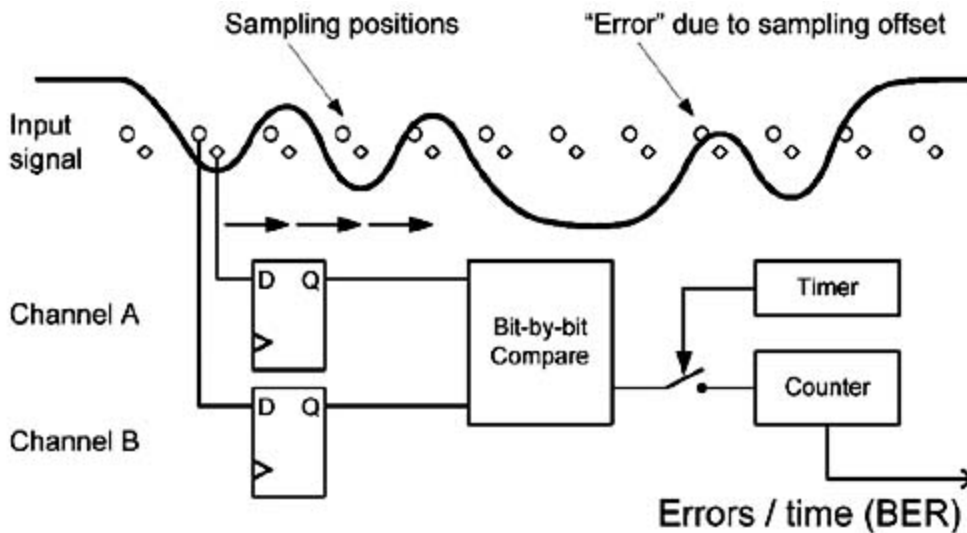


Figure 3. Results from sampling channel are compared and accumulated comparisons are collect to produce a bit-rate error like result.

The result obtained by the gated counter will reflect the respective locations of each sampling channel. As the displacement between the respective sampling positions increases, a point will be reached where some of portions of the input signal will cause a discrepancy between the two sampling channels.

As the displacement between the sampling channels is increased even further, the rate at which the two channels disagree will also increase. A systematic array of tests can be performed on the received waveform to produce a map of the voltage/phase characteristics of the signal as illustrated in **Figure 4** below:

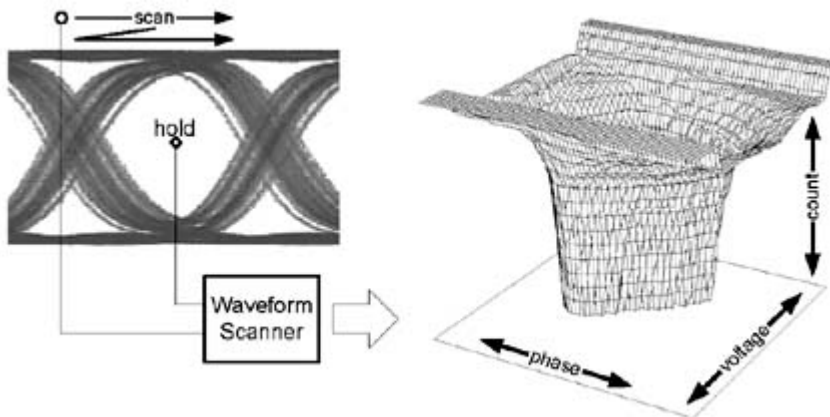


Figure 4. Tests performed on received waveforms produce a map of the voltage/phase characteristics of the signal.

Further processing of the data can produce eye diagrams that are very similar the type of waveform produced by a clock-triggered oscilloscope as shown in **Figure 5** below.

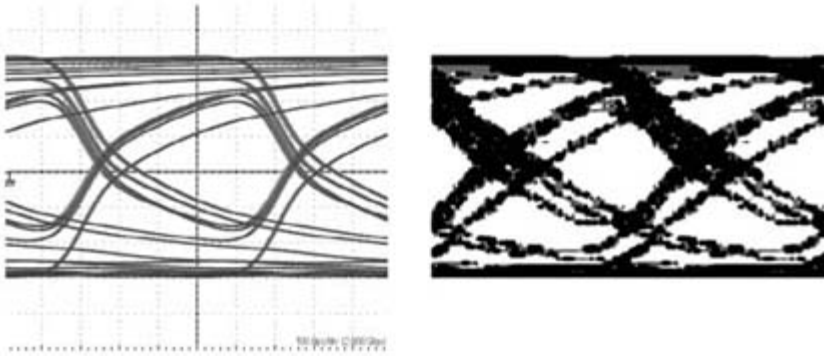


Figure 5. Oscilloscope view of test waveform, left, and data from wave form scan circuitry, left.

The scan represents not only the characteristics of the signal waveform, but also the acquisition characteristics of the decision circuit itself. The decision circuit (flip-flop) has finite frequency response characteristics that should be considered along with characteristics of the signal waveform itself.

What may appear as an acceptable waveform on a high-bandwidth oscilloscope may not be acceptable to the lower bandwidth of the decision circuit. By incorporating the characteristics of both into the data eye scan, a hybrid view can be obtained that has the attributes of both an analog oscilloscope and a bit-error rate tester.

The dual channel architecture assures exact correlation between the data gathered and the actual BER performance of the system. This is accomplished by always using one of the channels to carry the live data stream while the other channel scans. Once the scanning channel has determined its optimum location, it can trade places with the live channel so it can likewise scan and optimize.

The exchange between the two sampling channels can be performed without interrupting the data integrity, so that scans of the data eye can be performed on the live data stream on a continuous or on-demand basis.

When high-speed 1080i/1080p signals are aggregated in a common backbone, the monitoring function can enable new levels of efficiency in signal integrity debug and analysis.

VScope in a Video Application

In a large scale video router application, a router implements hundreds of multi-gigabit links in a matrix utilizing dozens of rack units. These routers are typically field-deployed in live broadcast environments where wiring complexity has scaled exponentially. The move to 3-Gbit/sec links creates new concerns with signal integrity. In this environment, real-time signal waveform viewing is a necessity.

A 3-Gbit crosspoint module used in these routers can take advantage of the crosspoint switch architecture by implementing embedded equalization for signal cleanup and utilizing a VScope transceiver such as the VSC3406. Any input or output pin in the switching module can then be monitored with a simple two-wire serial channel, in a manner unobtrusive to real-time traffic.

Using only one VSC3406, the entire module can be tuned and debugged for signal integrity, and a working system can be monitored remotely for ongoing "health checks." The solution can diagnose 1080i and 1080p video, at supported data rates up to 6 Gbits/sec.

Production switchers and backbone routers of the future will use a variety of switching and physical-layer transceiver IC architectures. But what is clear is that embedded real-time monitoring will fast become a necessity for the HDTV aggregation market.

Juan Garza is product marketing & applications manager at [Vitesse Semiconductor](#), and has experience in networking and communications including a variety of technology areas including digital signal processors, network processors, modem chipsets and DSL transceivers. He has a Bachelor of Science degree in Electrical Engineering from the University of Texas at Austin.

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